Opus DAC Manual
Twisted Pear Audio

Version 1.0

The Opus is a balanced output DAC based on the Wolfson WM8740. For detailed information about the WM8740 and its capabilities please refer to the data sheet here:

http://www.wolfsonmicro.com/uploads/documents/en/WM8740.pdf

This manual is geared toward using the DAC in hardware control mode with either stereo or mono differential (balanced) outputs. The Opus DAC can also be easily used in software mode, please refer to the data sheet for more information on software mode.

Once you have populated the PCBs you just need to set the jumpers and correctly wire the DAC to your power supply - such as an LCPS, wire analog outputs, and also wire your digital (I2S generally) source.

The Opus is designed to utilize separate analog and digital power supplies from 6.5V to 15V. They do not need to be regulated, but a good dual regulated supply like the LCPS is recommended. There are two on-board voltage regulators to provide power to the DAC. If you use the LCPS adjust both output voltages to 7.5V for good results. This will provide more than enough voltage drop for the on-board LDO VREGs while not making them dissipate more power than required.

On the PCB you will notice polarity markings next to the jumpers pins at either end of the line of jumpers. These mark the side on which you will put the jumper to make the input pin high(+) or low(G). The high side(+) is on the right when viewing the PCB with the text right side up.

Some of the pin headers like MUTE, RSTB could also be wired to a controller or switch. Refer to the data sheet. They have internal pull-ups to you do not need to jumper them at all if you do not want to. Not all the jumpers are required to be set.

To operate the DAC in dual differential(mono) mode you set the DIFFHW pin high. The MODE pin then set which channel the DAC will handle. MODE high = right, and MODE low = left. When the DAC is in differential mode the output pins are paralleled so that the DAC operates with lower distortion and noise.

IMPORTANT!!! In Dual differential mode you should use all of the output pins as described in this table. The pins are remapped and the polarity of the output is not the same as in stereo mode.

MONO LEFT (MODE = 0)

OUTPUT TERMINAL	OUTPUT SIGNAL
LEFT -	LEFT MONO -
LEFT +	LEFT MONO +
RIGHT +	LEFT MONO -
RIGHT -	LEFT MONO +

MONO RIGHT(MODE = 1)

OUTPUT TERMINAL	OUTPUT SIGNAL
LEFT -	RIGHT MONO +
LEFT +	RIGHT MONO -
RIGHT +	RIGHT MONO +
RIGHT -	RIGHT MONO -

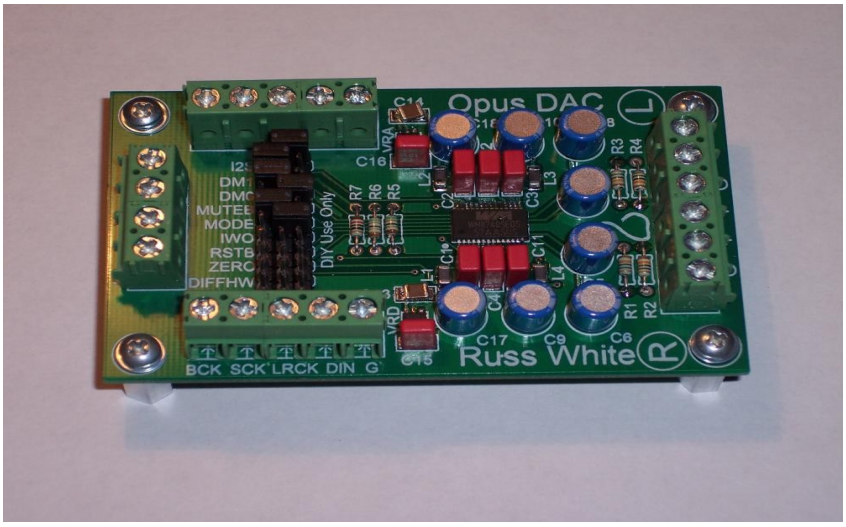

Figure 1, A populated DAC PCB setup for 24 bit I2S input and stereo output with no deemphasis. Notice just the first 6 jumpers are used.

PIN	NAME	TYPE	DESCRIPTION			
			Hardware Mode			Software Mode
			Normal Mode	Differential Mode	8X Mode	
23	CSBIWO	Digital input Internal pull-down	Wordlength: Low for 16-bit data. High for 20-bit (normal) or 24-bit I^2S data.	Wordlength: Low for 16-bit data. High for 20-bit (normal) or 24-bit I^2S data.	Wordlength: Low for 20-bit data. High for 24-bit data.	Low for serial interface operation.
24	MODE	Digital input Internal pull-up	Low for hardware mode.	Low for left mono mode. High for right mono mode	DINR	High for software mode.
25	MUTEB	Digital input Internal pull-up	Low to soft mute. High for normal operation.	Low to soft mute. High for normal operation.	Low to soft mute. High for normal operation.	Low to soft mute. High for normal operation.
26	MD/DM0	Digital input Internal pull-up	De-emphasis mode select bit 0.	Low for no de-emphasis. High for 44.1kHz de-emphasis.	LRP – LRCLK polarity select.	Control serial interface data signal.
27	MC/DM1	Digital input Internal pull-up	De-emphasis mode select bit 1.	Low for normal filter operation. High for filter slow roll-off.	Unused. Leave unconnected.	Control serial interface clock signal.
28	ML/I2S	Digital input Internal pull-up	Audio serial format: Low – right justified. High – I^2S.	Audio serial format: Low – right justified. High – I^2S.	Input data format: Low – right justified. High – left justified.	Control serial interface load signal.

Note: Digital input pins have Schmitt trigger input buffers.