Buffalo32S DAC

User Manual

Revision 2.0

Twisted Pear Audio

Overview

The Buffalo32S is a 32-bit stereo audio reference DAC module designed for uncompromising audio quality. Based on the ESS Technology ES9018 Sabre Reference chip, the Buffalo32S accepts S/PDIF, PCM, and DSD digital audio signal at sample rates up to 32-bit/192khz. The balanced stereo outputs are made up of four parallel DACs per channel.

Power Requirements

Recommended Supply Voltage	**Analog (VA)**	±15VDC
	Digital (VD)	+5VDC
Current Draw	**Analog (VA) (@ ±15V)**	~68mA (V+), ~43mA (V-)
	Digital (VD) (@ 5V)	~125mA

Configuration

Basic configuration of the Buffalo32S is performed using the DIP switches **SW1** and **SPDIF**.

SW1 is a four-position tri-state DIP switch with positions marked -, Open, and +, and switches numbered 1 through 4. Tables 1a and 1b show the effects of We recommend leaving the switches Open (middle position) or high(+) for default operation (S/PDIF or I2S/PCM input).

The tristate DIP switches are used to configure features of the DAC the DAC power should be cycled after changing these switches. See Tables 1a and 1b. It is suggested you leave these open (middle position) for default operation. The defaults were carefully chosen for best all-around performance. For SPDIF and PCM the defaults are ideal. For DSD you may want to change the IIR switch.

The **SPDIF** switch is used to connect D1 to the output of the SPDIF input comparator. It should be switched off when not using the SPDIF comparator such as when you plan on using PCM or DSD.

The **ADDRESS** header is used to select the I2C address of the DAC. You should leave the header open for the on-board controller to function correctly with the provided basic on-board firmware. Open uses the default address.

The **RESET** header is used to reset the DAC if necessary. This is not normally needed even when changing registers.

The **I2C** header is used to communicate with the DAC from a controller such as the Volumite.

DIP Switch 2	DIP Switch 1	DPLL Bandwidth
+	+	Lowest(best jitter rejection)
+	-	Medium_Low
-	+	Medium_High
-	-	Highest(fastest lock)

***Table 1a** - On-Board controller DPLL configuration.*

Switch	+	-
DIP Switch 3 – FIR Roll Off	Fast	Slow
DIP Switch 4 – IIR Bandwidth	Normal (Most linear response for PCM)	50Khz (Used for DSD)

***Table 1b** – On-Board controller FIR and IIR settings.*

Analog Characteristics

In the default configuration the balanced output at 0dbfs input will be ~4VRMS and you can take either OUT+ or OUT- and AGND for 2VRMS single ended.

There are 4 spots for optional resistors (R47 - R50) on the bottom of the PCB which allow you to reduce the output level if required. Table 2 shows some suggested values. The resistors should be good quality metal film with at worst 1% matching but .1% will produce less distortion. Values >= 287R are suggested for lowest distortion.

Value	Level
2K	2.0VRMS
1.2K	1.5VRMS
750Ω.	1.0VRMS
287Ω.	0.5VRMS

Table 2 *– R47-50 values and balanced output levels. Single ended levels are half the balanced levels.*

Using External Controllers

When using an external controller on the I2C bus (Volumite for example) it is required to remove the on-board controller otherwise the on-board controller will interfere with communication from the external controller.

Optional Features

The PCB has 4 marks near the outputs which when cut make the output impedance 21Ω. People using the DAC to drive headphones may wish to leave those uncut. Those using the DAC into capacitive cables and/or an amplifier will want to cut those traces where marked with red circles on figure 1. You will see the parallel lines on the PCB silkscreen that indicate where to make your cut.

There are also marked traces you can cut to use an external reference voltage for AVCC. The default reference is DVCC(3.3V) which is put through a thorough RC filter. Each of the two traces are marked with a blue X on figure 1. AVCC should be in the range of 3.3V +/- 5%. Voltage outside this range may result in damage the DAC. There are two pads on each side named “REF” and “AGND” for input.

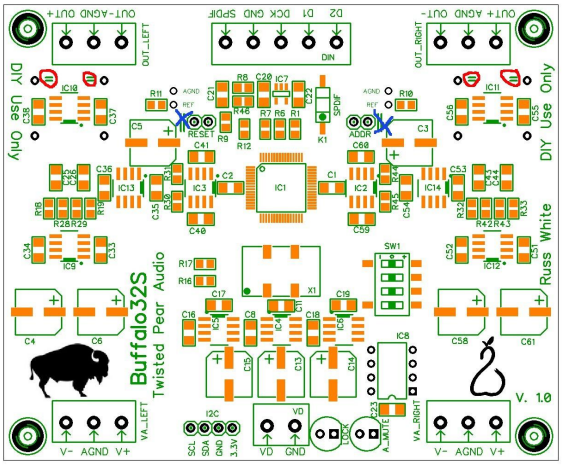

Figure 1

Connecting Digital Sources

Consumer Level SPDIF

Connect consumer level SPDIF signals to SPDIF and GND at the input terminal block. Make sure the SPDIF switch is closed.

TTL Level SPDIF

Make sure the SPDIF switch is open. Connect TTL level SPDIF signals to D1 and GND at the input terminal block.

TTL Level I2S

Make sure the SPDIF switch is open. Connect I2S signals as follows:

Source GND → GND

Source Bit Clock → DCK

Source Word Clock(LRCK) → D1

Source Data → D2

TTL Level DSD

Make sure the SPDIF switch is open. Connect DSD signals as follows:

Source GND → GND

Source Bit Clock → DCK

Source Data 1(usually left) → D1

Source Data 2(usually right) → D2

Ballsie Lite

We also have designed a stereo balanced to single ended converter which will get you slightly better dynamic range than using just one end of the balanced outputs. That module is called the “Ballsie Lite”. It also has a shunting relay which eliminates any turn-off thump. For single ended users wanting the highest DNR this would be the ideal choice. You can also mount this module on the bottom of the DAC similar to what I did for “Thump Buster” but it will be offset to one side as it is a single board.